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(54) Digital to analogue converter

(57) A D/A converter is followed by a low-pass filter. To convert the digital signal values with a small amount of circuitry to an analogue signal that permits high-quality reproduction (e.g. stereo sound), the D/A converter is preceded by a coding circuit which transforms the digital signal values into pulse packets (22) each consisting of a number of pulses following each other without interruption. The repetition rate of these pulse packets is a multiple of the repetition rate of the signal values. The pulse packets (22) are largely symmetrical with respect to centerlines (ML) spaced at equal time intervals. A pulse on one and/or the other side of the centerline (ML) has an amplitude smaller than or equal to a maximum value, and all other pulses of the pulse packet (22) have the maximum value. The voltage-time area of each pulse packet (22) corresponds to the respective digital signal value.

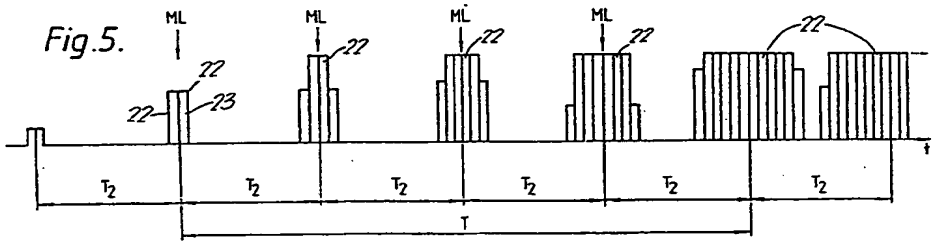

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Fig.1.

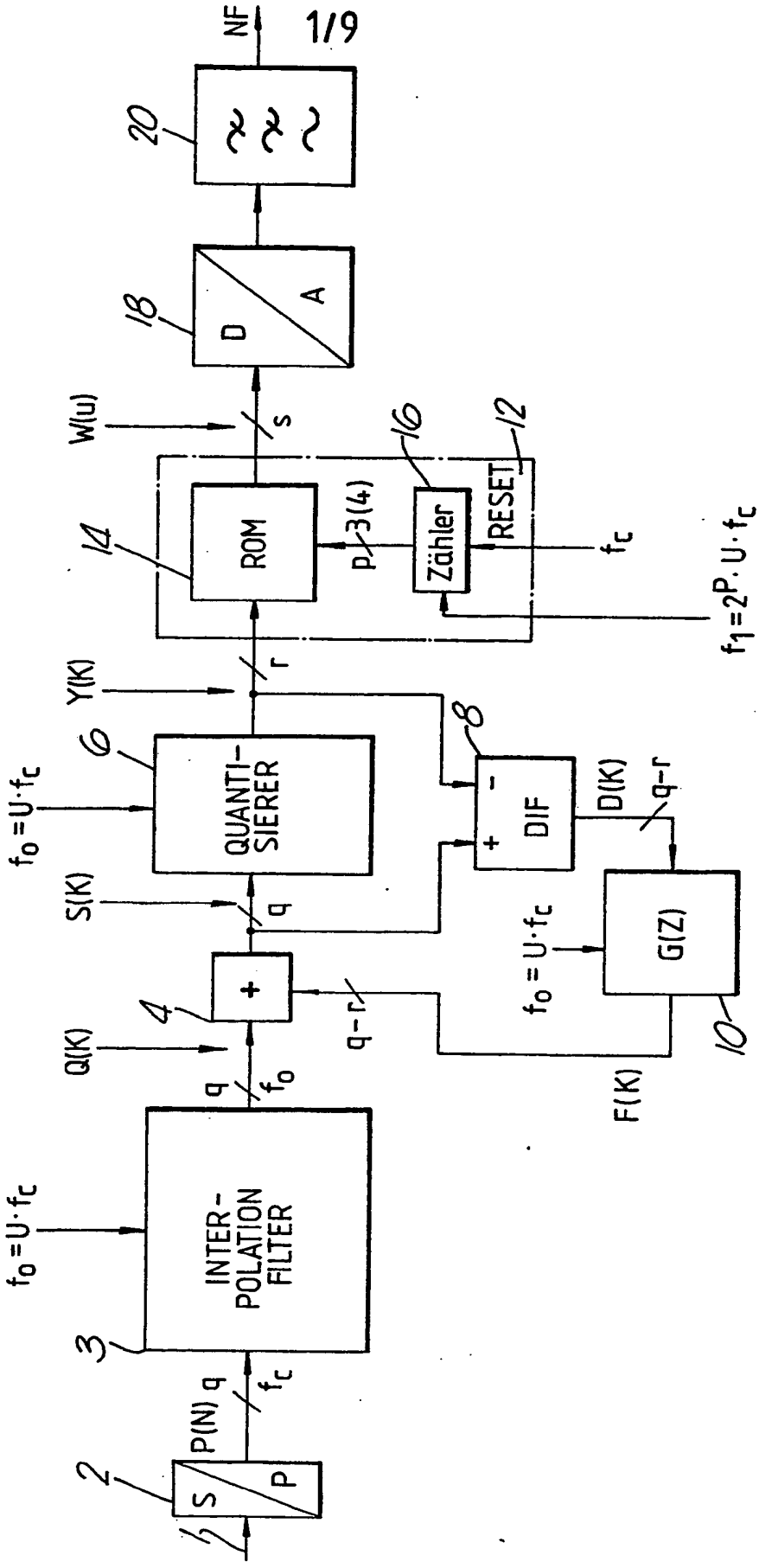

Fig. 2.

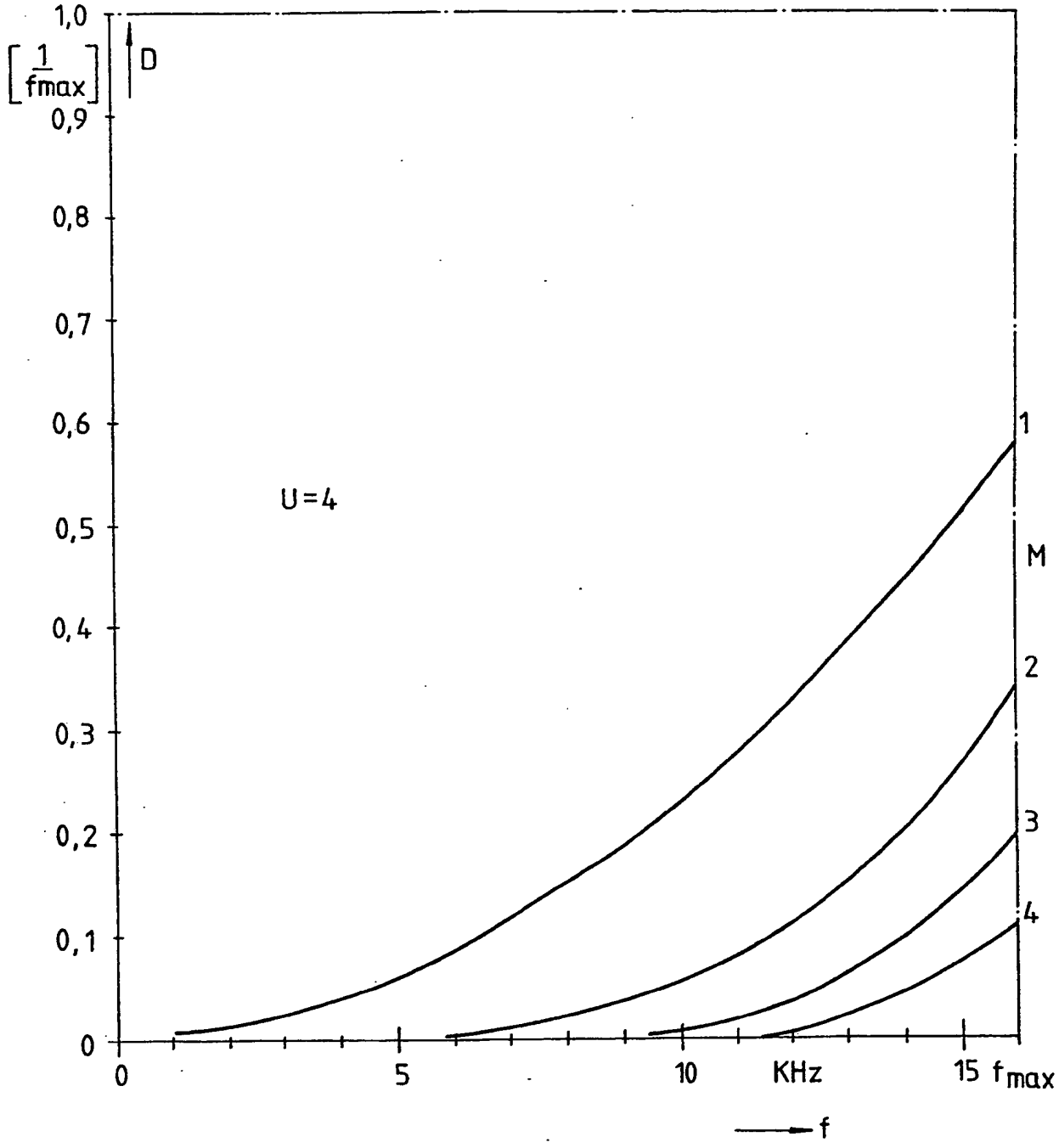

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Fig.3.

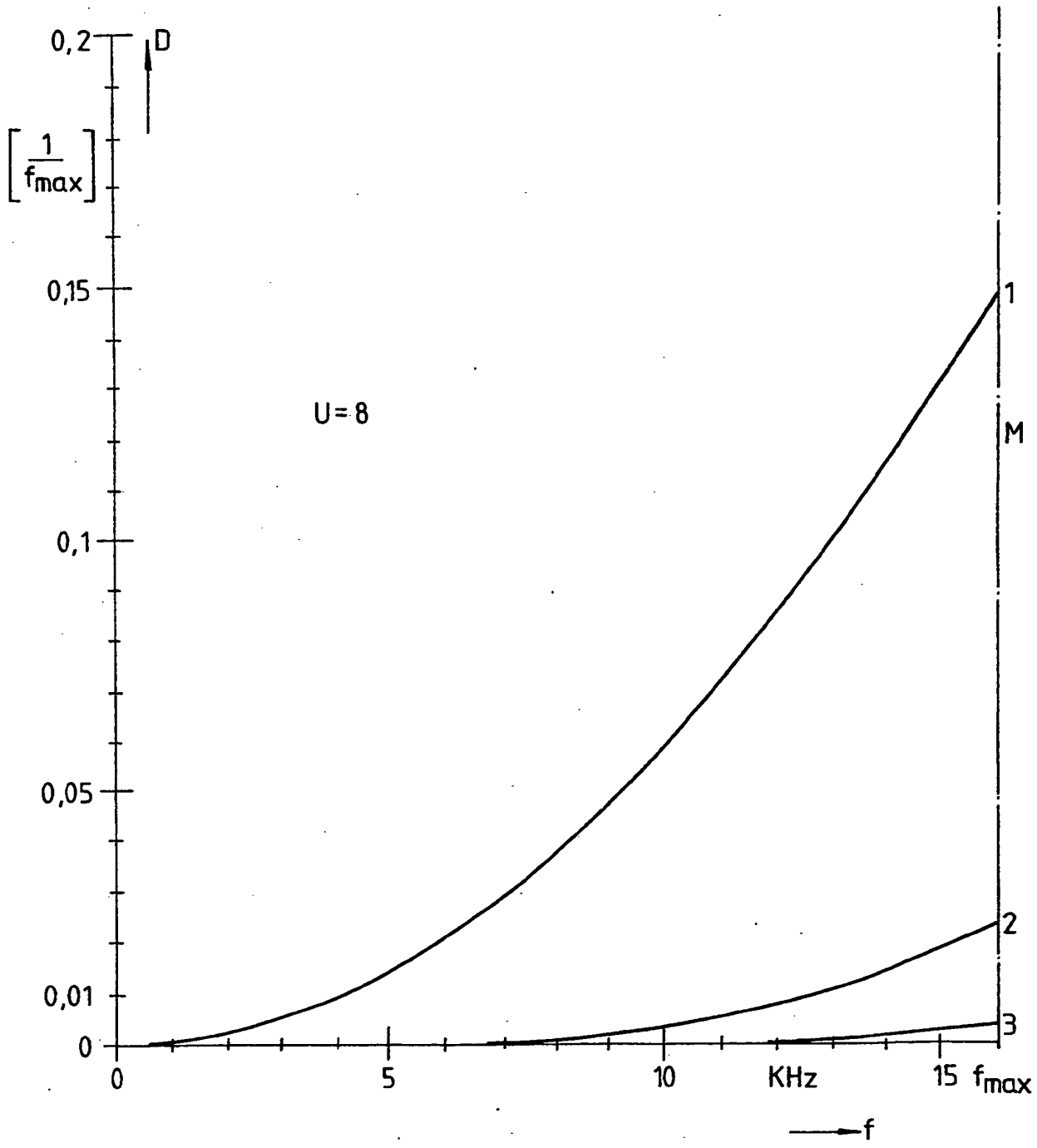
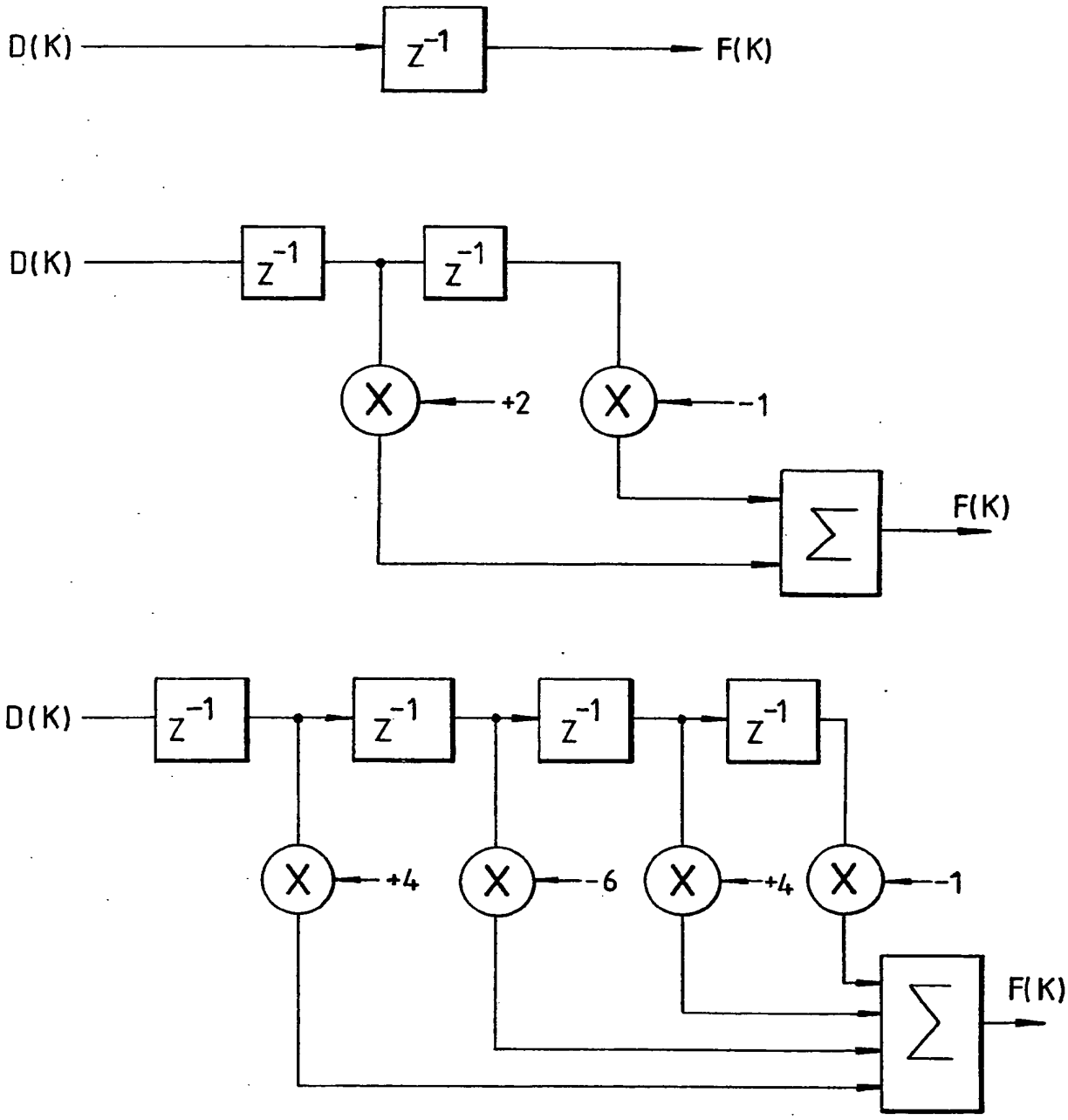


Fig. 4.



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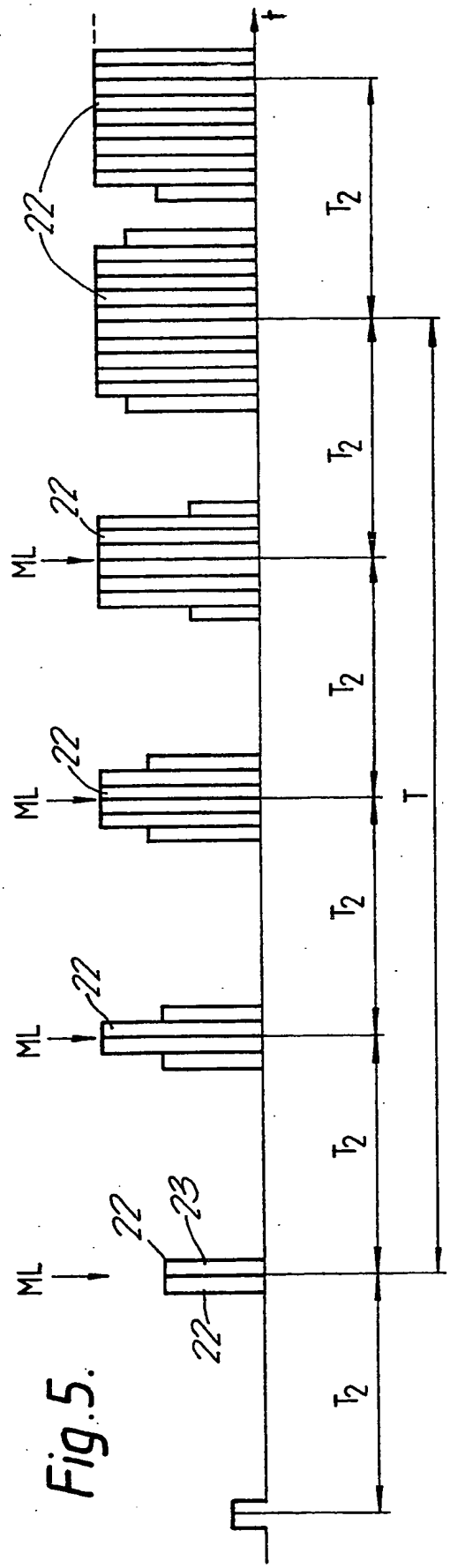


Fig.5.

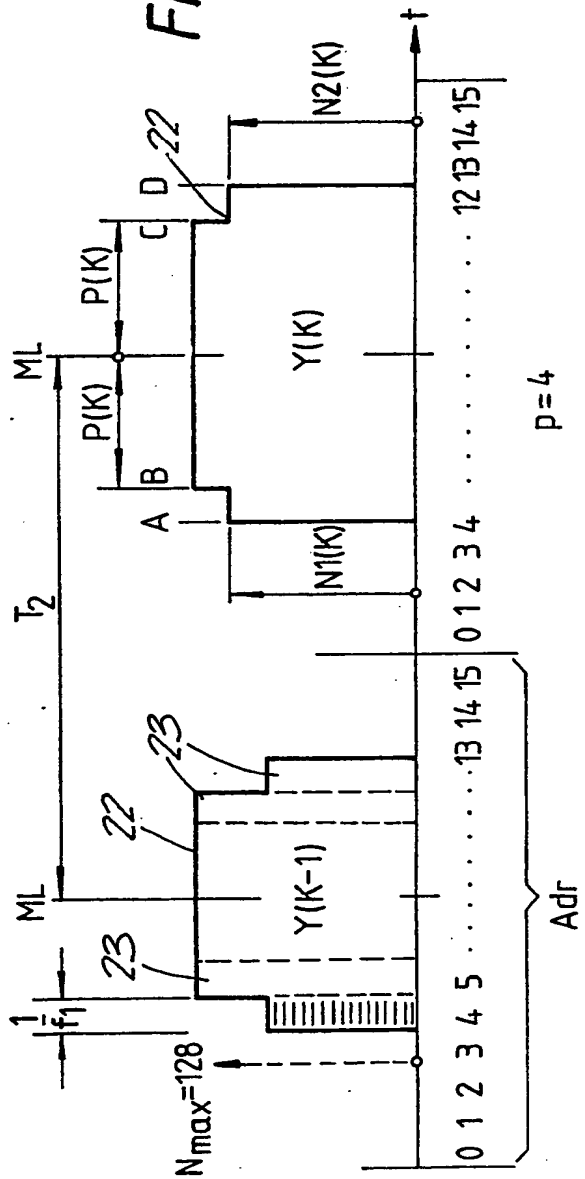


Fig.6.

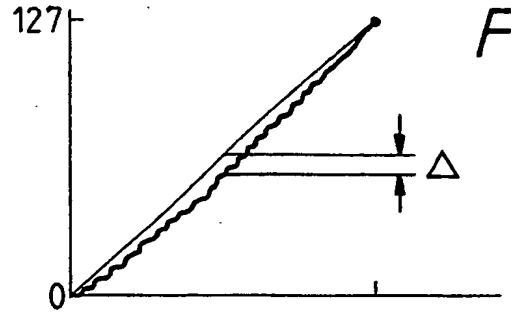


Fig.7a.

Fig.7b.

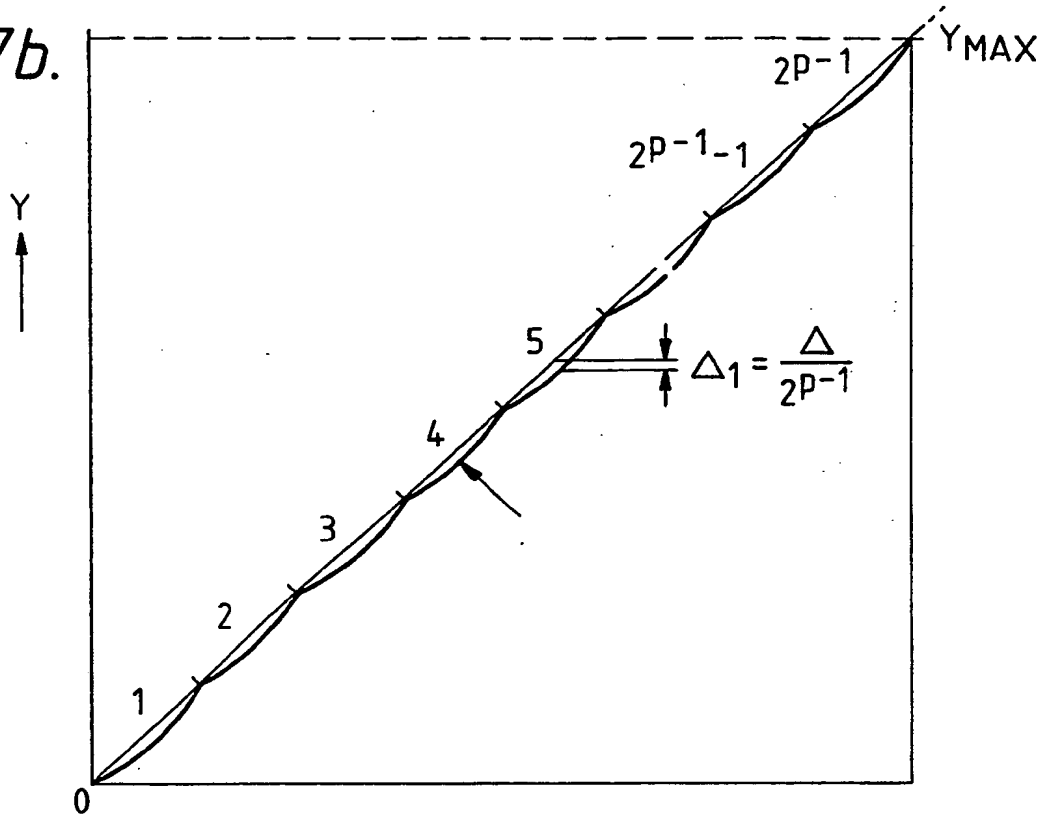


Fig.7c.

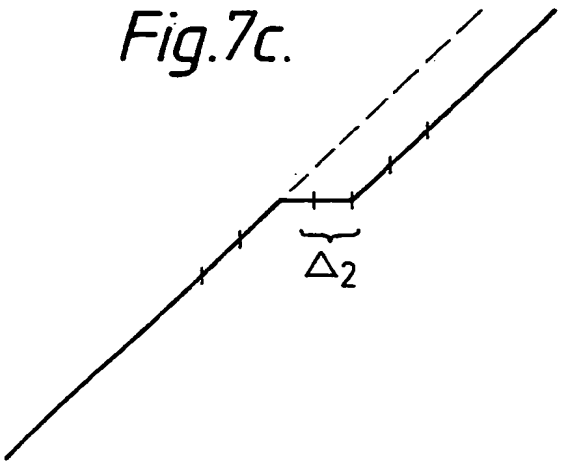
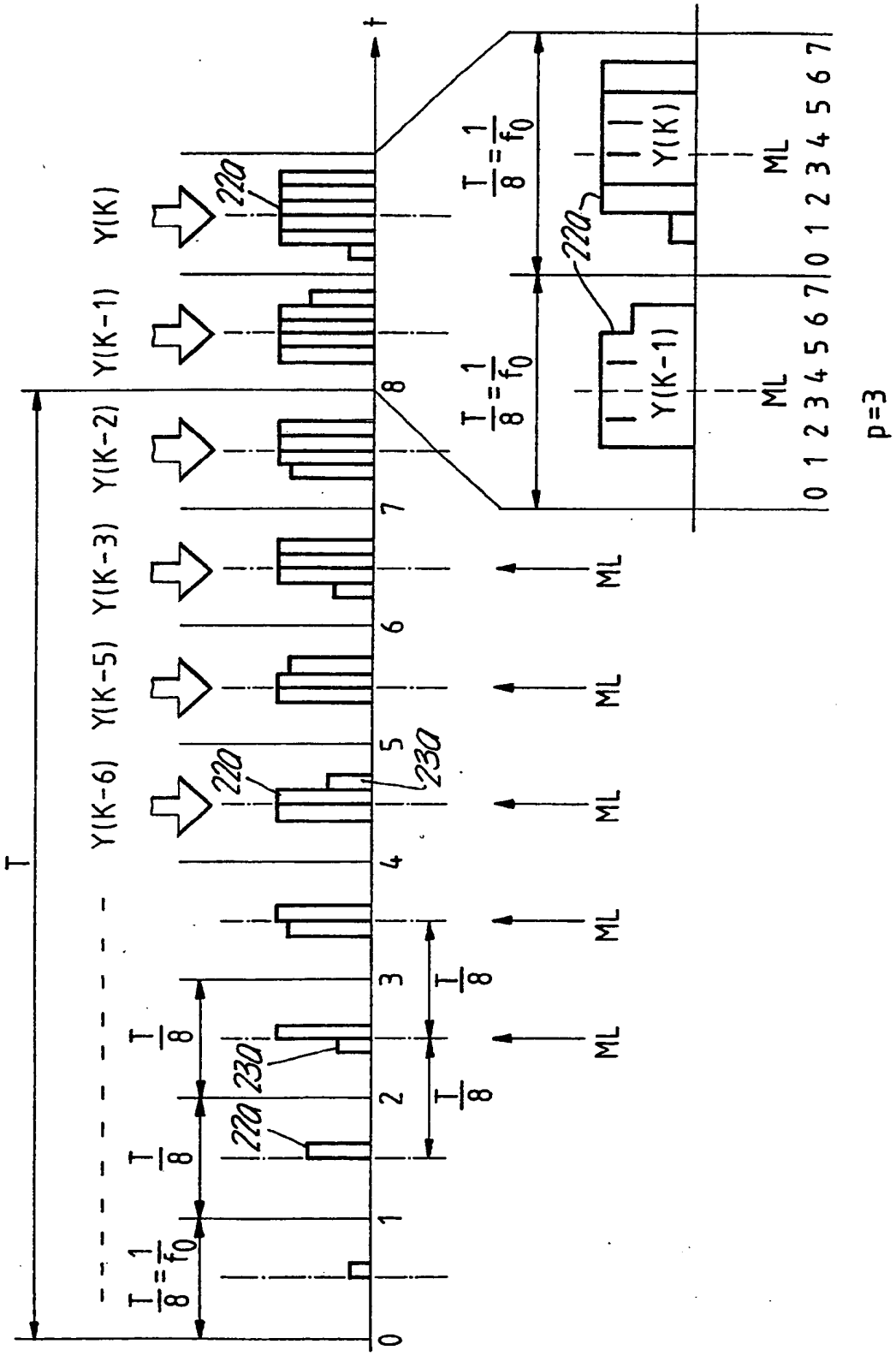


Fig.8.



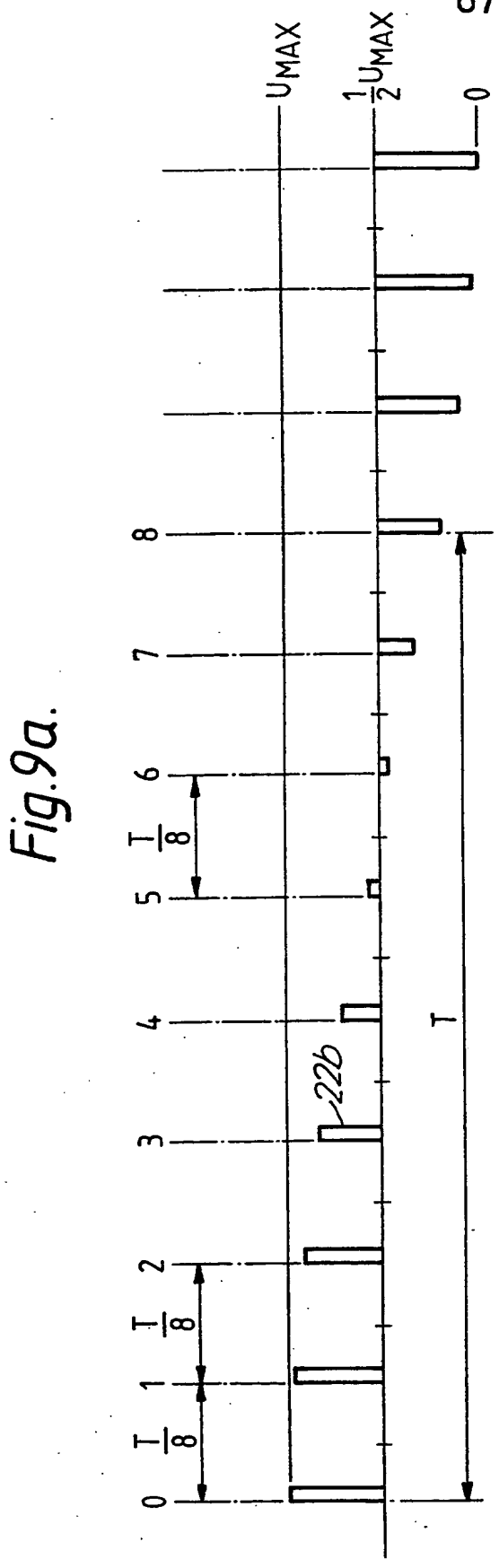


Fig.9a.

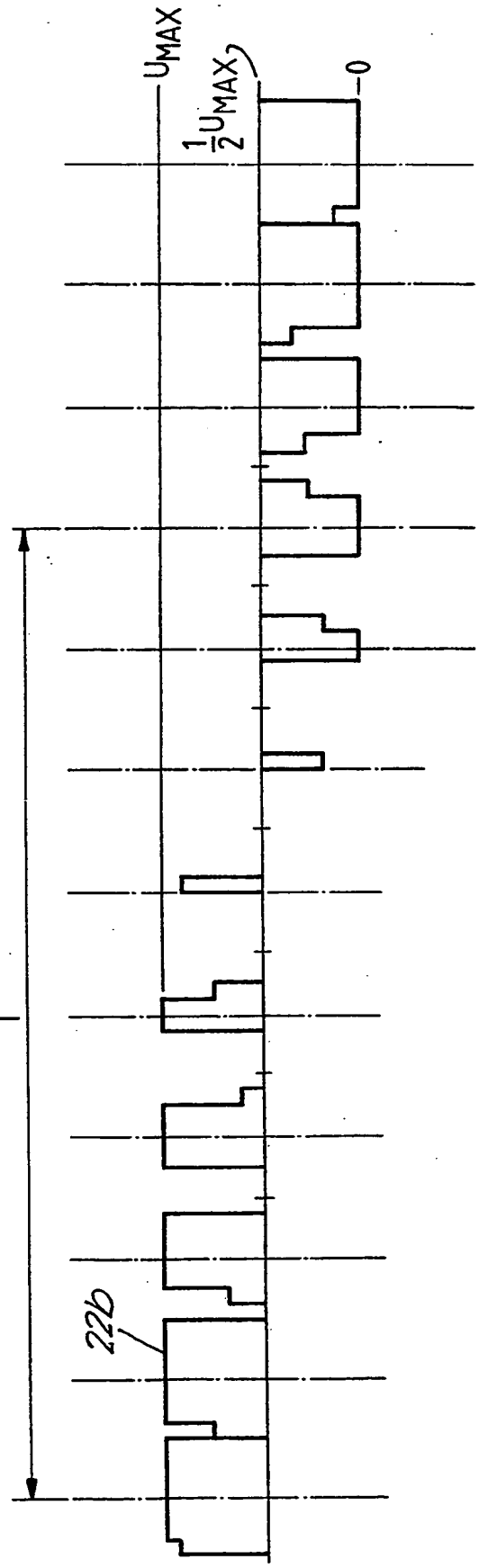
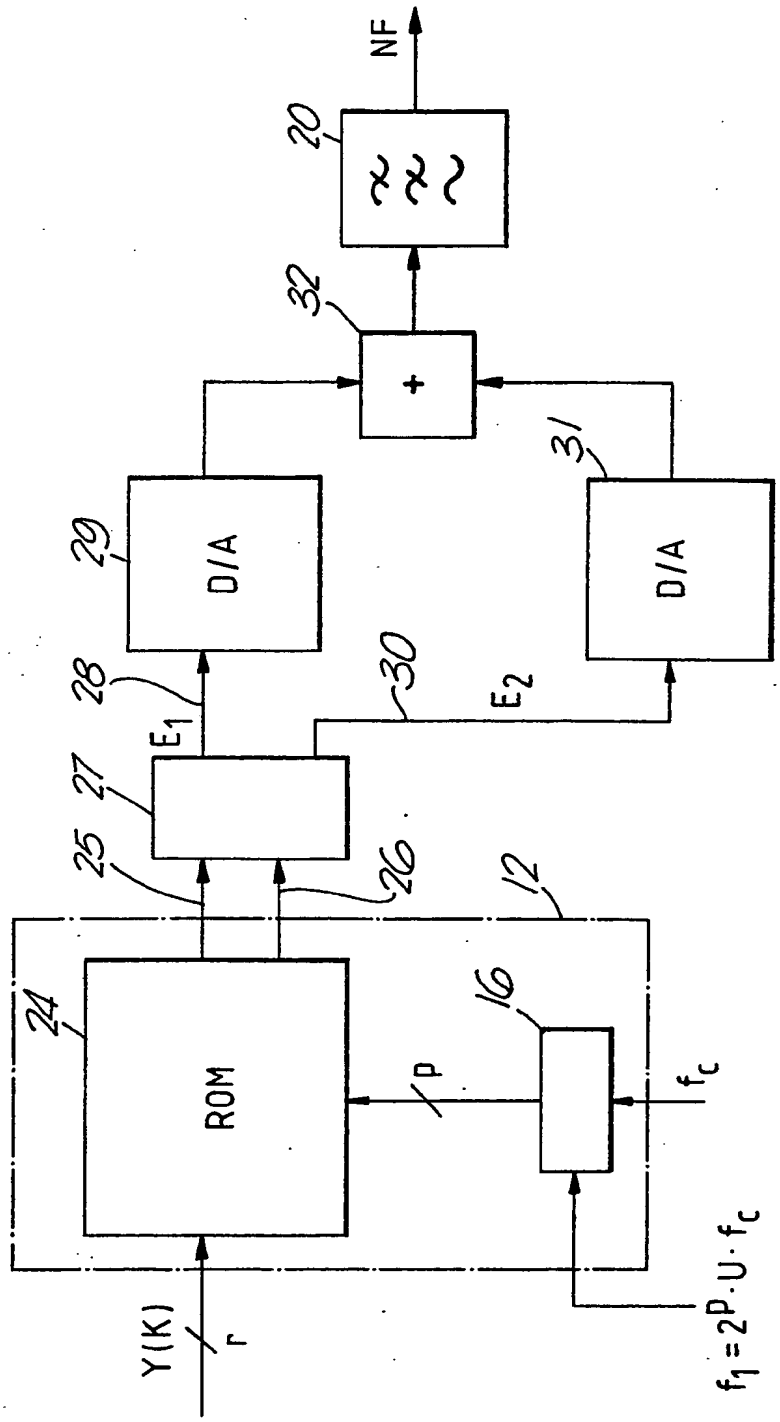


Fig.9b.

Fig. 10.



SPECIFICATION

Digital to analogue converter circuit arrangement and method of digital to analogue convertion

The present invention relates to digital to analogue convertion in which low pass filtering is effected after convertion. Such a procedure may permit signals which were originally analogue signals, e.g. audio signals, and which have been digitised, e.g. by pulse-code modulation, – for better transmission in a telecommunication network, to be converted back at a receiver into analogue signals necessary for reproduction.

In the planned broadband integrated-services digital network, BISDN, stereophonic signals of high quality are to be transmitted. To digitise such signals, finer quantisation levels must be used, so that each transmitted sample value has a word length of, e.g. 15 bits. To convert the digital signal values back into analogue audio signals prior to reproduction at the receiver, 15-bit digital-to-analogue (D/A) converters are needed which meet stringent linearity requirements. Such D/A converters, however, are extremely expensive to fabricate.

In a prior art D/A converter (British Patent 1 444 216), the sampling rate of the incoming digital values is therefore increased, and the word length of the signal values is reduced. A pulse stream is produced whose mean density is proportional to the signal amplitude. From this pulse stream, the analogue signal can be reconstructed by means of a low-pass filter. To process high-quality stereophonic signals, however, a high sampling frequency of 32 kHz is required, which, in the prior art converter, results in very high pulse repetition rates (8 to 16 MHz) and, thus, in an equally high system clock frequency if 15-bit amplitude quantisation is used. In addition, a very-high-precision pulse shaper is necessary before the analogue postfiltering to make the area of the pulses constant, taking account of leading and trailing edges. Such a pulse shaper, however, is of complicated design and difficult to implement.

The present invention seeks to convert digitised signals to an analogue signal with a small amount of circuitry and in such a way that high-quality reproduction is possible.

According to one aspect of the invention there is provided a digital to analogue circuit arrangement comprising a digital-to-analogue converter followed by a low-pass filter, characterised in that the digital-to-analogue converter is preceded by a coding circuit in which the digital signal values are transformed into pulse packets which consist of a number of pulses following each other without interruption and having a repetition frequency equal to a multiple of the repetition frequency of the signal values, that the pulse packets have a shape which is largely symmetrical with respect to equidistant centerlines, that a pulse on one and/or the other side of the centerline of the pulse packet has an amplitude smaller than or equal to a maximum value, while all other pulses of the pulse packet have the maximum value and that the time integral over a pulse packet corresponds to the digital signal value at the input of the coding circuit.

The invention also includes a method for converting a digital signal to an analogue signal employing such a converter comprising the following steps: increasing the repetition frequency of the incoming signal values by interpolation, reducing the word length of the signal values of increased repetition frequency, deriving an error signal from the difference between the interpolated signal values of increased repetition frequency and the signal values having a reduced number of bits and the same repetition frequency, band limiting the error signal by digital filtering adding the band limited error signal to the signal values of increased repetition frequency, converting the signal values of increased repetition frequency to an analogue signal, and suppressing the clock-frequency components by analogue postfiltering, characterised in that the signal values having a reduced number of bits and increased repetition frequency are converted to pulse packets of the same repetition frequency which are symmetrical with respect to instants following each other at the increased repetition frequency, and that the time integrals of the amplitudes of the individual pulse packets correspond to the amplitudes of the incoming digital signal values.

The circuit of the invention is well suited for integration. Where clock frequencies of about 512 kHz to 2048 MHz are employed, these can be readily implemented with MOS technology. A D/A converter with a maximum word length of 8 bits is suited for implementation in MOS technology, too, because it need not meet any stringent linearity requirements. The amount of circuitry required for analogue postfiltering is extremely small because of the oversampling.

In order that the invention and its various other preferred features may be understood more easily, some embodiments thereof will now be described, by way of example only, with reference to the drawings, in which:-

Figure 1 is a block diagram of a digital to analogue converter in accordance with the invention,

Figure 2 is a graph showing the relative power density of the noise signal, reduced by quantisation-error feedback, with fourfold oversampling,

Figure 3 is a graph showing the relative power density of the noise signal, reduced by quantisation-error feedback, with eightfold oversampling,

Figure 4 shows three embodiments of error filter which can be used in the converter of Figure 1,

Figure 5 shows a first form of signal pulses delivered by the converter of Figure 1,

Figure 6 shows details of the signal pulses of Figure 5,

Figures 7a, 7b and *7c* are graphs illustrating the linearity improvement achieved by the invention,

Figure 8 shows a second form of signal pulses delivered by the converter of Figure 1,

Figure 9 shows a third form of signal pulses delivered by the converter of Figure 1,

Figure 10 shows a modification of a portion of the converter of Figure 1.

Figure 1 shows a transmission line 1, which for example forms part of a BISDN network, over which PCM-coded stereophonic signals are transmitted to a digital-to-analogue converter, constructed in accordance with the invention, where they ar converted to analogue signals. The D/A converter forms part of a terminal which is connected to the n twork and with which the received stereophonic signals are reproduced via loudspeakers.

The digital signal or sample values arriving serially on the line 1 are fed to a serial-to-parallel converter 2, in which they are converted to parallel form with a word length of q bits. In the embodiment, q = 15; accordingly, the transmission line has q parallel wires. The sequence of incoming sample values is denoted in Figure 1 by P(N), where N is the sequence index.

The sample values P(N) are received at a repetition rate of f_C = 32 kHz. In an interpolation filter 3, they are converted to an interpolated signal-value sequence Q(K) with the same quantisation q but at a repetition rate f_O increased by an oversampling factor U.

The output of the interpolation filter 3 is connected via an adder stage 4 to the input of a quantiser 6. In the quantiser 6, the signal values S(K) from the adder stage 4, which arrive as parallel word containing q = 15 bits and will be explained below, are reduced in words length, so that r-bit parallel words (e.g. r= 11) are provided at the output.

In a subtracter 8, a quantisation-error sequence D(K) is formed by subtracting the output signals Y(K) of the quantiser 6 from the input signals S(K). In the embodiment, the quantisation-error values consist of the separated least significant bits of S(K). In an error filter 10, feedback values F(K) are derived from the quantisation-error values D(K). They are added in the adder stage 4 to the output-signal values Q(K) from the interpolating filter 3 to obtain the input-signal values S(K) for the quantiser 6. If the error filter 10 has a suitable time response, the quantisation-error feedback, which is known per se, causes that component of the quantisation noise spectrum in the output signal Y(K) of the quantiser 6 which lies in the audible range to be shifted toward higher frequencies, i.e. outside the audible range.

To a first approximation, it can be assumed that the quantisation noise of a D/A converter corresponds to white noise and is not correlated with the input signal. The quantisation gives a noise signal Y_{St} which adds to the useful signal Y_{Nutz} at the output of the quantiser. through the feedback of the quantisation error to the input of the quantiser 6, one obtains

$$Y = Y_{Nutz} + [1 - G(Z)]*Y_{St}$$

where $Z = e^{j2\pi\frac{f}{f_o}} = \cos(2\pi\frac{f}{f_n} + j.\sin(2\pi\frac{f}{f_o})$

f = noise frequency

$f_O = U*f_C$ = out put rate of $Y_{(K)}$

The relative noise amplitude is

$$\frac{Y - Y_{Nutz}}{Y_{St}} = \frac{Y'_{St}}{Y_{St}} = 1 - G)Z)$$

If a simple delay element (Z^{-1}) is used for the error filter, then

$$\frac{Y'_{St}}{Y_{St}} = 1 - Z^{-1}$$

An error filter of degree M can be implemented, for example, by setting

$$1 - G(Z) = [1 - Z^{-1}]^M$$

It can be shown that the relative power density D of the corrected noise signal is then given by

$$D = \frac{1}{f_{max}} * 2^{2M} * \sin^{2M}(\pi.\frac{f}{U.f_C})$$

In Figures 2 and 3, the relative power density D of the corrected n ise signal is plotted against frequency, with the filter degree M as a parameter. Figure 2 holds for an oversampling factor of U = 4, and Figure 3 for an oversampling factor of U = 8. The scale factor $1/f_{max}$ of the ordinate corr sponds to the noise signal of a D/A converter without quantisation-error feedback. In Figure 3, this scal value lies outside the drawing because of the enlarged ordinate scale.

From Figures 2 and 3 it can be seen that the area bel w the curves and, thus, the power density of the noise

signal e rapidly with increasing ov rsampling factor U and increasing filter degree M.

For M U=4, the improvement in signal-to-noise ratio resulting from the quantisation-error treatment and thampling amounts to 18.6 dB + 6dB = 24.6 dB. For M=2 and U=8, the improvement is already 23.3 dB + 9 dB. The word length of the sample values may be reduced by one bit per 6 dB improvement. In the firsthe reduced word length is only 11 bits instead of 15 bits, and in the second case only 10 bits.

Accto the power-density spectra illustrated in Figures 2 and 3, a considerably greater word-length reductil would be possible. In deriving the power-density spectra, however, it is assumed that the quantisnoise is not correlated with the useful signal. This assumption is only conditionally true, however. Particuat a very low noise level, there is such a correlation, which limits the word-length reduction. Therefhe curves of Figures 2 and 3 and the signal-to-noise improvements derived therefrom can only be regard coarse estimates. They are only to illustrate the trend. If M=4, the equation for the filter type propo is

$$-G(Z) = [1-Z^{-1}]^4$$

$$= 1-4Z^{-1}+6Z^{-2}-4Z^{-3}+Z^{-4}$$

$$G(Z) = 4*Z^{-1}-6Z^{-2}+4Z^{-3}-Z^{-4}$$

Figure 4 shows three embodiments of such error filters, namely a filter of degree 1 at the top, and filter of degree 2 in the middle, and a filter of degree 4 at the bottom.

The sample-value sequence Y(K) at the output of the quantiser 6 (Figure 1) could be provided via a commercially available D/A converter with correspondingly reduced quantisation, but this D/A converter would have to have a very high linearity. Such D/A converters are very expensive to manufacture and are not suited for MOS or CMOS integration.

The invention makes it possible to use D/A converters with lower linarity and lower resolution.

The output of the quantiser 6 is connected to the input of a coding circuit 12. In the latter, the signal-value sequence Y(K) is transformed into a value sequence W(U) increased by the factor 2^p, which, after being converted from digital to analogue form and low-pass-filtered, forms the analogue output signal NF.

The coding circuit 12 contains a read-only memory (ROM) 14, in which a code conversion is performed according to a rule to be explained below, and a counter 16, which provides the addresses for the ROM 14. The counter 16 has a word length of p bits, i.e. it has p parallel outputs. In the embodiment, p = 3 or 4. If the word length of the signal values Y(K) is r bits, it is reduced in the coding circuit 12 to s bits, where s=r−p.

The counter 16 is clocked at a frequency

$$f_1 = 2^p * f_0 = 2^p * U * f_C$$

and reset at the frequency f_C.

The signal values presented at the output of the coding circuit 12 are transferred to a d/A converter 18. The output of the latter provides pulse packets 22, which are shown in Figures 5 and 6.

The pulse packets 22 are composed of voltage pulses 23 of frequency f_1. Each pulse packet is symmetrical about a vertical centerline ML. the centerlines are spaced

$$T_2 = \frac{1}{U*f_C}$$

apart.

The packet repetition rate is thus equal to the repetition rate of the sample values Y(K), and the time integral of the voltage pulses – in the representation f Figures 5 and 6 the voltage-time area of a pulse packet – corresponds exactly to the digital signal value Y(K).

The pulse packet shown, 22, correspond to an over-sampling factor of U=4. The period corresponding to the input repetition frequency f_C is thus

$$T = 4*T_2$$

The low-pass filter 20 following the output of the D/A converter 18 suppresses the sampling frequency

$$\frac{1}{T_2} = 128\,kHz$$

The pulse output of the d/A converter according to the invention is a mixed pulse-amplitude-pulse-width modulation, with the pulse width being quantised, too. Figure 5 shows pulse packets 22 whose area increases from left to right. Only the two outer pulses $N_1(K)$ and $N_2(K)$ of a pulse packet (Figure 6) are amplitude-modulated, while the pulses 23 have the maximum amplitude. The number of inner pulses of the pulse packet is 2*P(K).

The signal value Y(K) is represented by the values 0 to 10.

$$Y(K) = Y_{10}Y_9Y_8Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$$

P(K) $N_1(K)$,

i.e. P(K) is represented by the three most significant bits Y_{10} to Y_8, and

$N_1(K)$ by the bits Y_7 to $_1$.

If, for example, a pulse consists of $2^7 = 128$ sub-areas, and the maximum number of pulses of a packet is $2^p = 16$, the geometry of the pulse packet can be represented in a simple manner:

$N_{max} = 128$

$P(K) = Y_{10}Y_9Y_8$ (three most significant bits)

$N_1(K) = Y_7Y_7...Y_1$

$N_2(K) = N_1(K)$ if $T_0 = 0$

$N_2(K) = N_1(K) + 1$ if $Y_0 = 1$

In the ROM 14 of the coding circuit 12, the pulse heights corresponding to the signal values Y(K) are stored in locations 0 to 15, whose addresses are formed by the counter 16. The latter, as mentioned above, is clocked at the frequency f_1 and reset at the frequency f_c. Since, with such a simple law for forming the individual signal-amplitude values W(U), the code table in the ROM 14 shows great redundancy, the ROM 14 may be replaced by a PLA (programmable logic array) device, which requires considerably fewer locations.

Figure 7a shows the linearity error of a conventional D/A converter, the error having the form of a sagging curve. This curve is transversed repeatedly with increasing AF amplitude as the outer pairs of bars of the pulse packet 22 grow. This results in a repeated image of the curves of Figure 7a as shown in Figure 7b. Referred to the final value Y_{max}, the linearity error with this form of signal output is reduced to

$$\Delta_1 = \frac{\Delta}{2^{p-1}}$$

where p = number of bits of the counter 16

2^{p-1} = maximum number of pairs of bars per pulse packet.

Figure 7c shows an additional nonlinearity Δ_2 in the form of a step error, which, according to the formation law just explained, is caused by the fact that, in an n-bit D/A converter, for example, a bar has n height steps but only n−1 sub-areas between the height steps.

The following table 1 illustrates this problem in the binary number system.

TABLE 1

Y(K)	P(K) $Y_{10}Y_9Y_8$	N1(K) $Y_7...Y_1Y_0$
⋮		
257	001	00000001
256	001	00000000
255	000	11111111
254	000	11111110
253	000	11111101
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
5	000	00000111
4	000	00000100
3	000	00000011
2	000	00000010
1	000	00000001
0	000	00000000

TABLE 2

Y(K)	P(K) $Y_{10}Y_9Y_8$	N1(K) $Y_7 \ldots Y_1 Y_0$
255	001	00000001
254	001	00000000
253	000	11111101
252	000	11111100
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-
5	000	00000101
4	000	00000100
3	000	00000011
2	000	00000010
1	000	00000001
0	000	00000000

A signal value N1(K) reaches its maximum numerical value already at Y(K) = 254, and cannot be further increased at Y(K) = 255. At the signal value Y(K) = 256, the high-order bit group P(K) increases from binary 000 to 001, so that, according to the formation law explained above, the maximum bar height of $N1(K)_{max} = 127$ is set again. At the three signal values Y(K) = 254, 255 and 256, the bar height is thus equal to 127. The monotonous increase of the function is thus disturbed over two positions, as can be seen from Figure 7c.

The additional non-linearity can be eliminated by adding a bit representing the 128th height step to the word length of the D/A converter 18. Within the range of validity of the bit group P(K), the D/A converter 18 then outputs the value 10000000_2. if the value $N1(K) = 1111111_2$, and $Y_0 = 1$, this highest-order current source will be activated an additional time at the right-hand partial pulse $N_2(K)$.

This has the disadvantage that, to represent only one missing quantisation step, the accuracy of the DA converter must be increased by a factor of 2 (one additional bit). To avoid this disadvantage, the base of the number system is changed from 2^{s+1} to $2^{s+1}-2$, where s = word length of the D/A converter.

In the present embodiment, where s = 7, the base of the number system is reduced from 256 to 254. This is illustrated in table 2. The carry from P(K) = 0 to P(K) = 1 takes place at Y(K) = 254. Again.

$N_2(K) = N_1(K)$ if $Y_0 = 0$, and

$N_2(K) = N_1(K) + 1$ if $Y_0 = 1$

Thus, if $Y_{(K)} = 253$, then $N_{1(K)} = 126$ and $N_{2(K)} = 127$.

If $Y_{(K)} = 254$, then $N_{1(K)} = N_{2(K)} = 0$, but $P_{(K)} = 1$, whereby an innner pair of bars is set to the maximum value 127. For $Y_{(K)} = 255$, a new outer pair of bars begins because $N_{1(K)} = 0$, and $N_{2(K)} = 1$. The area of the pulse packet 22 thus increases continuously.

The total representable number of steps $Y(K)_{max}$, however, is reduced from $16 \times 128 = 2048$ to $16 \times 127 = 2032$. The AF dynamic range is thus reduced by about 8%. This, however, is practically negligible. The base conversion is stored also in the form of an allocation table in the ROM 14.

Another advantage of the conversion of signal values to pulse packets lies in the fact that this prevents the occurrence of undesired voltage spikes in the D/A converter 18. These are generally caused by delay differences in the current switches of the D/A converter, particularly if the latter switch alternately, between the digital values 1000000 and 0111111. This causes transient currents which result in undesired spikes – also known as "glitches" – in the analogue signal and, thus, impair the signal-to-noise ratio of the entire circuit.

Part of the current sources of the D/A converter are turned on at point A of the pulse packet 22 (Figure 6, at the right), and the remainder of the current sources are turned on at point B. At point C, only part of the current sources are turned off, and at point D, the remainder of the current sources are turned off.

Alternate turn-on and turn-off can occur only at a very high AF input level if two successive pulse packets follow each other without interruption. This case is statistically very rare, however. In addition, th undesired noise thus caused is then masked by the high loudness level. Figure 8 shows a s cond pulse output form. In each of th pulse packets 22a, unlike in the pulse packets 22 of Figure 6, only one outer bar increases in h ight with continuously increasing amplitude, this amplitude-modulated bar 23a adjoining alternately the right- and left-hand sides of the puls packet. Despite this asymmetry, the centres of the pulse packets 22a remain largely equidistant. the time error is greater than with the pulse output form of Figures 5 and 6 but still small compared with the period T of the AF cycle.

The maximum time error is

$$\Delta t_{max} \leq \frac{1}{2.f_1} = \frac{1}{2^{p+1}U.f_c}$$

where 2^p is the maximum number of pulses per pulse packet.

The following relation holds:

$$\frac{\Delta t_{max}}{T_{NF}} = \frac{f_{NF}}{2^{p+1}.U.f_c}$$

At an audio frequency of $f_{NF} = \frac{1}{4} * f_C = 8$ kHz,

$$\frac{\Delta t_{max}}{T_{NF_{min}}} = \frac{1}{2^{p+3}.U}$$

If an oversampling factor of U = 8 and a count length of p = 3 are chosed as in the case of the pulse packets of Figure 8, the maximum time error referred to the AF period is only 0.2%. The distortion factor is small compared with this time error and, thus, negligible. The advantage of this pulse output form over that of Figures 5 and 6 lies in the fact that, for the same factor U and the same word length p, the number of partial curves (cf. Figure 7b) doubles. the linearity error, referred to the maximum output, level is thus halved, i.e.

$$\Delta_1 = \frac{\Delta}{2^p}$$

On the other hand, with an unchanged linearity requirement, the oversampling factor U can be doubled without having to double the output pulse repetition frequency f_1. As explained above, this reduces the word length r of the value sequence Y(K) to, e.g. 10 bits, and the resolution s of the D/A converter to 7 bits. The address range p + r of the ROM 14 is reduced by 2 bits.

To eliminate the need for an additional bit in the D/A converter to represent the 2^sth sub-area of a bar, the base of the number system can again be converted by means of an allocation table in the memory 14 or a PLA device. Since individual bars rather than pairs of bars are constructed here in succession, the base must be reduced from 2^s to 2^s-1.

Figure 9 shows a third output form of pulse packets 22b. The pulses are symmetrical with respect to a reference voltage of, e.g. $1/2*U_{max}$. Depending on the sign of the amplitude of the AF signal, the pulses, referred to the reference voltage, are positive or negative. Figure 9a shows the zero crossing of an AF wave of small amplitude. It can be seen that there is no time error at low AF input levels. The time error occurs only at large amplitudes, at which it is neutralised by the well-known masking effect. A zero crossing of an AF wave of large amplitude is shown in Figure 9b.

Here, a particular advantage is that, at small amplitudes, also the harmonic content produced by the sampling frequency is small. The ratio of the harmonics to the amplitude of the AF signal is thus largely constant. The analogue low-pas filter 20 can therefore be chosen to be of a lower degree than with the first pulse output forms. The formation rule for the third pulse output form, too, is stored in the form of an allocation table in the ROM 14.

With a 7-bit D/A converter, for example, the centerline $1/2\ U_{max}$ corresponds to the digital value 1000000_2, for example. After the zero crossing of the AF wave, the digital value is slightly smaller, e.g. 0111111. However, this transition, as mentioned above, results in an undesired transient voltage spike because in this case all current sources of the D/A converter switch at the same instant.

Such voltage pulses can be avoided with the arrangement of Figure 10. In this arrangement, the coding circuit 12 includes a ROM 24 whose two outputs are connected to a gate circuit 27 by lines 25 and 26, respectively. Of the output data of the memory 24, the absolute value is fed to the gate circuit 27 over the line 25, and the sign over the line 26. The outputs of the gate circuit 26 are connected to a first D/A converter 29 by a line 28, and to a second D/A converter 31 by a line 30. Each of these D/A converters 29, 31 has half the resolution of the D/A converter 18 of Figure 1. The outputs of the two D/A converters 29, 31 are added in a summing circuit 32, and the sum is fed to the low-pass filter 20, whose output provides the AF signal.

If the sign is positive, the gate circuit 27 applies the absolute value over the line 28 to the input of the first D/A converter 29, and the highest absolute value 111111_2 as a fixed value over the line 30 to the input of the second D/A converter 31. If the sign is negative, the gate circuit negates the absolute value bit by bit, i.e. it forms the binary complement and feeds it to the second D/A converter 31, while all bits transf rr d over the line 28 to the first D/A converter 29 ar changed to logic 0.

To eliminate th n ed for the additional bit required in the present example to represent the 2^6th sub-area, in the embodiment of Figure 10, too, the base of the number system can be changed from $2^6 = 64$ to $2^6-1 = 63$, preferably also by means of an allocation table stored in the ROM 24.

CLAIMS

1. A digital to analogue circuit arrangement comprising a digital-to-analogue converter followed by a low-pass filter, characterised in that the digital-to-analogue converter is preceded by a coding circuit in which the digital signal values are transformed into pulse packets which consist of a number of pulses following each other without interruption and having a repetition frequency equal to a multiple of the repetition frequency of the signal values, that the pulse packets have a shape which is largely symmetrical with respect to equidistant centerlines, that a pulse on one and/or the other side of the centerline of the pulse packet has an amplitude smaller than or equal to a maximum value, while all other pulses of the pulse packet have the maximum value and that the time integral over a pulse packet corresponds to the digital signal value at the input of the coding circuit.

2. A circuit arrangement as claimed in claim 1, characterised in that the coding circuit contains a read-only memory and a counter which addresses the read-only memory.

3. A circuit arrangement as claimed in claim 1, characterised in that the pulses are constructed by the coding circuit alternately on both sides of the centerline of the pulse packet.

4. A circuit arrangement as claimed in claim 3, characterised in that the pulse packets are composed of pulses in the form of bars arranged in pairs about the centerline.

5. A circuit arrangement as claimed in claim 1, comprising an interpolating filter in which the digital signal values received at a first repetition frequency are changed into signal values of increased repetition frequency, a quantiser in which the number of parallel bits constituting the individual signal values is reduced, an error filter in which quantisation-error values are formed from the difference between the input- and output-signal values of the quantiser and fed back to the input of the quantiser, a digital-to-analogue converter in which the signal values delivered by the quantiser are converted to an analogue signal, and a low-pass filter which suppresses the sampling-frequency components in the analogue signal, characterised in that between the output of the qantiser and the input of the digital-to-analogue converter, a coding circuit is inserted in which the output signal values of te quantiser are transformed into pulse packets of the increased repetition frequency, that said pulse packets are symmetrical with respect to instants following each other at the increased repetition frequency, and that the time integral of the amplitudes of each of the pulse packets corresponds to the amplitudes of the digital signal values of increased repetition frequency.

6. A circuit arrangement as claimed in claim 2, characterised in that the counter is clocked at a frequency which is greater than the repetition frequency of the output-signal values of the quantiser by a factor of 2^p, where the number p is equal to the number of outputs of the counter, and that the counter is reset at the repetition frequency of the incoming signal values.

7. A circuit arrangement as claimed in claim 1, characterised in that the coding circuit has two outputs connected via a gate circuit to the inputs of a first digital-to-analogue converter and a second digital-to-analogue converter, and that the outputs of the digital-to-analogue converters are connected to a summing unit.

8. A circuit arrangement as claimed in claim 7, characterised in that the signs of the output-signal values and the absolute output-signal values of the coding circuit are transferred to the gate circuit over a first line and a second line, respectively, that, if the sign is positive, the absolute value is fed to the first digital-to-analogue converter, and the highest possible absolute value (1111111_2) to the second digital-to-analogue converter, and that, if the sign is negative, the absolute value is negated bit by bit and fed to the second digital-to-analogue converter, while the first digital-to-analogue converter is presented exclusively with zero bits.

9. A digital-to-analogue circuit arrangement substantially as described herein with reference to the drawings.

10. A method for converting a digital signal to an analogue signal using a circuit arrangement as claimed in any one of the preceding claims, comprising the following steps: increasing the repetition frequency of the incoming signal values by interpolation, reducing the word length of the signal values of increased repetition frequency, deriving an error signal from the difference between the interpolated signal values of increased repetition frequency and the signal values having a reduced number of bits and the same repetition frequency, band limiting the error signal by digital filtering adding the band limited error signal to the signal values of increased repetition frequency, converting the signal values of increased repetition frequency to an analogue signal, and suppressing the clock-frequency components by analogue postfiltering, characterised in that the signal values having a reduced number of bits and increased repetition frequency are converted to pulse packets of the same repetition frequency which are symmetrical with respect to instants following each other at the increased repetition frequency, and that the time integrals of the amplitudes of the individual pulse packets correspond to the amplitudes of the incoming digital signal values.

11. A method as claimed in claim 9, characterised in that the repetition frequency of the digital signal values is increased by an oversampling factor of 2 to 8.

12. A method for converting a digital signal to an analogue signal substantially as described h rein with reference to the drawings.

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